## Remarks

Claims 1, 3, 4, 7, 10-18, and 20 are pending in this application. Claims 2, 5, 6, 8, 9, and 19 were previously cancelled. The Office action rejected claims 1, 4, and 6 under 35 U.S.C. § 103(a) as being unpatentable by U.S. Patent Publication No. 2003/0046464 to Murty et al. (hereinafter "Murty") in view of U.S. Patent No. 4,370,720 to Hyatt (hereinafter "Hyatt"). Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Murty in view of U.S. Patent No. 5,809,314 to Carmean et al. (hereinafter "Carmean"). Further, claims 7, 8, 10-15, 17, 19, and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Murty in view of Hyatt and further in view of U.S. Patent No. 6,857,084 to Giles (hereinafter "Giles"). Finally, claims 16 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Murty/Hyatt in view of Giles, and further in view of Carmean. In this response, claim 1 is amended.

### A. Remarks Regarding Rejection of Claims 1, 3, and 4 Under 35 U.S.C. § 103

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The Office action states:

> The Examiner notes that the processors of Murty are "operable "to be serially released and "operable" to initiate the release and no teachings of Murty preclude operability and do not stipulate that the "operable" steps of the claim limitations cannot be accomplished by the prior art.
>
> Furthermore, in order to assist the applicant to better understand the rejection of the claim limitation "serially released" the

> Examiner points to paragraph 0027. The system of Murty consists of multiple processors arranged from 120(1) to 120(n) each associated with a thread. Consequently the order of operation for tasks handled by all the processors will also occur in the same 1 to n order. In paragraph 0027 and 0049 Murty teaches that each logical processor from 1 to n will execute a first code segment in consecutive order, which will bring it into the interrupt mode. During the interrupt handling mode the first processor will initiate a flag as seen in paragraph 0034 and handle the interrupt and exit. The next processors will serially execute the first code segment and check the flag for interrupt handling and serially will be released in consecutive order 1 to n, by the interrupt handler as seen in paragraph 0027 and 0049.

(Office action, 3-4) Applicant disagrees. Applicants agree that Murty discusses logical processors 120(1) to 120(n). Murty does not make any disclosure, however, that "consequently the order of operation for tasks handled by all the processors will also occur in the same 1 to n order," as the Office action suggests. For example, in the cited paragraph [0027], Murty states that "[t]he first of logical processors 120 that successfully accesses ICR 150 completes processing of the interrupt, and remaining logical processor 120 resume execution of their threads." This is a race allocation of interrupts to logical processors, not a serial allocation as the Office action suggests. Nor is any such disclosure of a serial allocation inherent in the disclosure of Murty. To the contrary, Murty teaches against such an allocation: "[t]he present invention provides a mechanism that allows one logical processor 120 to execute the full interrupt-handling routine for an interrupt . . . **without imposing asymmetries on logical processors 120, such as arbitrarily assigning interrupts to logical processor 120**." (Murty, [0026])

Applicants further disagree with the Office actions assertion that "during the interrupt handling mode the first processor will initiate a flag as seen in paragraph 0034 and handle the interrupt and exit. The next processors will serially execute the first code segment and check the flag for interrupt handling and serially will be released in consecutive order 1 to n, by

the interrupt handler as seen in paragraph 0027 and 0049." As discussed above, the first of Murty's logical processors to respond to an interrupt handles the interrupt. Neither paragraphs 0027, 0049, nor any other paragraph of figure in Murty disclose that "the interrupt handling processor assigned to perform the processing tasks associated with the interrupt **initiates the release of the non-interrupt handling processors from the interrupt mode on a timed release basis following the completion by the interrupt handling processor** of the processing tasks associated with the interrupt," as required by claim 1. Murty states in 0027 that "[t]he first of logical processors 120 that successfully accesses ICR 150 completes processing of the interrupt, **and the remaining logical processors 120 resume execution of their threads**." Thus, execution of threads **during** the handling of an interrupt is encompassed in Murty's disclsoure. As such, there is absolutely no disclosure that the non-interrupt handling processors are released after the competition of the interrupt by the interrupt handling processor, as required by the claim. Even if such a disclosure were made explicitly or inherently by Murty, which Applicant does not concede, Murty makes no disclosure of releasing the non-interrupt handing processors (1) in a serial manner and (2) on a timed release. Nor is any disclosure inherent in Murty. To the contrary, Murty's logical processors may and will most likely return to thread processing in a non-sequential order because "[t]he first logical processors 120 that successfully accesses ICR 150 completes processing of the interrupt, and remaining logical processors 120 resume execution of their threads."

With respect to the Office actions suggestion that "no teachings of Murty preclude operability and do not stipulate that the 'operable' steps of the claim limitations cannot be accomplished by the prior art." Applicant disagrees. First, Applicant has made clear in this response that claimed information handling system must actually be **configured** to perform the

claimed limitation. Furthermore, the absence of a teaching that the prior art cannot be configured as claimed is not legally equivalent to an explicit or inherent disclosure that the prior art is configured according to the claim, as required by §§ 102/103. The Office action must rely on the explicit or inherent disclosure of the prior art. The Office action cannot resort to constructing the Applicant's invention out of the prior art which replying on hindsight bias.

The purported combination of Murty and Hyatt fails to teach or suggest all the claim limitations of independent claim 1. Specifically, the combination fails to teach or suggest that "the interrupt handling processor assigned to perform the processing tasks associated with the interrupt **initiates** the release of the non-interrupt handling processors from the interrupt mode." Rather, Murty teaches that one of the logical processors is the first to access the shared register and handles the interrupt. Murty at [0049]. The rest of the "logical processors detect that the interrupt has been claimed and return from the interrupt-handler." Murty at [0049]. Murty does not disclose that the first processor "initiates" the release of the other processors. Murty teaches that the other processors detect that another processor is handling the interrupt and "return" from the interrupt handler. Murty at [0049].

Murty also fails to disclose a "timed release basis" for releasing the non-interrupt handling processors so as to release them from the interrupt mode serially. Murty discloses resetting a flag and merely states that the "time between common interrupts is typically greater than the time necessary for all of the logical processors to execute the interrupt handler ... and access the flag." Murty at [0046]. Murty does not mention a time delay between releasing processors. The time referenced in Murty relates to the time between typical interrupts and *not* the time delay associated with releasing the non-interrupt handling processors so as to reduce contention for system resources as required by independent claim 1.

Further, Murty does not disclose the successive serial release of logical processors from the interrupt mode "so as to reduce contention by the non-interrupt handling processors for system resources" as required by claim 1. Examiner states that the "order of operation for tasks handled by all the processors will also occur in the same 1 to n order" where 1 to n is the label given to the processors to indicate that more than one processor is contemplated. Office Action at 4. However, Murty does not discuss the processors registering a common interrupt for logical processors 120(1) - 120(n) in any particular order nor does it discuss releasing them in any particular order. Murty denotes that element 120 is a processor and identifies that any number of processors can exist by labeling the processors with the common notation of (1) to (n). Murty at Figure 1. In fact, Murty discloses that any processor could be the first processor to access ICR 150 and complete the processing of the interrupt. Murty at [0027]. Murty merely states that after the first processor has accessed the ICR 150 the remaining processors "resume execution of their threads." Murty at [0027]. Murty states that "[t]he remaining logical processors read the second value, which directs them to exit the interrupt-handler." Murty at [0049]. Murty does not discuss that these processors are released serially or that they will be released in consecutive order. In fact, the processors cannot be released in a pure consecutive order as any of the 1 to n processors could be the processor that is handling the interrupt. Murty even discloses that "each processor, acting independently, [determines] whether or not it is responsible for handling the common interrupt." Murty at [0034]. Murty describes this handling of interrupts as a "race-to-flag mechanism" and does not require that the processors act consecutively or serially. Murty at [0034].

Also, Hyatt does not disclose non-interrupt handling processors being serially released as required by claim 1. Hyatt is directed to "a numerical control system for machine

control using a stored program data processor; particular for coordinate resolution of motion commands." Hyatt at 3:6-9. Hyatt describes the operation of a data processor for performing micro-operations. Hyatt at 19:46-55. The processor responds to a series of flip-flops that indicate the next micro-operation. Hyatt at 19:66-20:25. For instance, an X5 signal indicates that an external interrupt has occurred, whereupon the data processor ignores it unless certain flip-flops are in certain states. Hyatt at 18-25. The cited portion of Hyatt by Examiner does not discuss a non-interrupt handling processor at all. The description in Hyatt of a data processor responding to flip-flops is not the same as the requirements of claim 1.

Because all of the elements of independent claim 1 are not taught or suggested by the combination of Murty and Hyatt, a prima facie case of obviousness is not established. In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Here, regardless of whether it is proper to combine the teachings of Murty and Hyatt, all of the claimed limitations of independent claim 1 are not shown in the combination. Applicant respectfully submits that the rejection of claim 1 should be withdrawn and that this claim should be passed to issuance. Claims 3 and 4 each depend directly or indirectly from independent claim 1 and are therefore requested to be passed to issuance for at least the same reasons.

**B. Remarks Regarding Rejection of Claims 7, 8, 10-15, 17, 19, and 20 Under 35 U.S.C. § 103**

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA

1970). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The combination of Murty and Hyatt in view of Giles fails to teach or suggest all the claim limitations of independent claims 7 and 17. Specifically, Murty in view of Hyatt in further view of Giles fails to teach "**initiating the serial exit** of the non-interrupt handling processors from interrupt mode" as required by claims" as required by claim 17 and similarly by claim 7 for at least the same reasons stated above with respect to claim 1. As discussed above, in Murty, the logical processor that services an interrupt provides does nothing to release the other processors. Instead, the other logical resume processing threads **even while the interrrupt-servicing processor is servicing an interrupt.** Thus, Murty teaches away from the limitation that "for the interrupt handling processor, **following the completion of the processing tasks necessary to resolve the interrupt condition, initiating the serial exit of the non-interrupt handling processors from interrupt mode**, whereby contention by the non-interrupt handling processors for control of the processor bus is reduced." In Murty, the "processing tasks necessary to resolve the interrupt" could be handled simultaneously with the processing of other threads. Murty therefore does not disclose this limitation. Hyatt and Giles fail to compensate for the deficiencies in Murty.

With respect to claims 11, 12, and 17, Giles fails to disclose "determining whether each non-interrupt handling processor was in a halt state immediately before entering the mode." Giles discusses that processors are placed in a debug mode "without an excessive time delay to preserve the states of the processors for multiprocessor debug by **halting all of the processors at approximately the same time**." Giles at 2:32-35. Giles teaches placing every processor in the halt state regardless of the prior state. This is not the same as determining if a "non-interrupt

handling processor was in a halt state immediately before entering the mode" as required by these claims.

Because all of the elements of independent claims 7 and 17 are not taught or suggested by the combination of Murty in view of Hyatt in further view of Giles, a prima facie case of obviousness is not established. In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Here, regardless of whether it is proper to combine the teachings of Murty and Hyatt, all of the claimed limitations of independent claims 7 and 17 are not shown in the combination. Applicant respectfully submits that the rejection of claims 7 and 17 should be withdrawn and that these claims should be passed to issuance. Claims 10-16, 18, and 20 each depend directly or indirectly from independent claims 7 and 17 and are therefore requested to be passed to issuance for at least the same reasons.

**C. No Waiver**

All of Applicant's arguments and amendments are without prejudice or disclaimer. Additionally, Applicant has merely discussed example distinctions from the cited references. Other distinctions may exist, and Applicant reserves the right to discuss these additional distinctions in a later Response or on Appeal, if appropriate. By not responding to additional statements made by examiner, Applicant does not acquiesce to examiner's additional statements, such as, for example, any statements relating to what would be obvious to a person of ordinary skill in the art. The example distinctions discussed by Applicant are sufficient to overcome the anticipation rejections.

## Conclusion

Applicant respectfully submits that the pending claims 1, 3, 4, 7, 10-18, and 20 of the present invention are allowable. Applicant respectfully requests that the rejection of the pending claims be withdrawn and that these claims be allowed.

Respectfully submitted,

/Bradley S. Bowling/
Bradley S. Bowling
Registration No. 52,641

Baker Botts L.L.P.
910 Louisiana St.
One Shell Plaza
Houston, Texas 77002-4995
(713) 229-1707

Baker Botts Docket Number: 016295.1472

Date: April 13, 2008